Conference Agenda

19th Electronics Packaging Technology Conference

Date: Wednesday, 06/Dec/2017

Time	Session		
7:00am - 8:30am	**PDC Registration**		
8:30am - 12:00pm	**PDC 1: Electronic Packaging for 5G Microwave and Millimeter Wave Systems IEEE by Dr. Rick Sturdivant** Location: Paradiso Room	**PDC 2: Automotive electronics – requirements and reliability by Dr. Mervi Paulasto-Kröckel** Location: Cardinal Room	**PDC 3: MEMS Fabrication: from theory to packaging by Dr. Liu Aiqun** Location: Swallow Room
12:00pm - 1:30pm	**Lunch**		
1:30pm - 5:00pm	**PDC 4: Fan-Out Wafer-Level Packaging and 3D Packaging by Dr. John H Lau** Location: Paradiso Room	**PDC 5: Reliability from a Semiconductor Suppliers Perspective by Dr. Stevan Hunter** Location: Cardinal Room	**PDC 6: Advanced LED packaging technology and reliability by Dr. Ricky Lee** Location: Swallow Room
5:30pm - 7:30pm	**Panel Session: Packaging Challenges & Opportunities of 5G-mm Wave Technology** Location: Galleria Ballroom		
7:30pm - 10:00pm	**Dinner: VIP**		

Date: Thursday, 07/Dec/2017

7:45am - 8:30am — Conference Day 1: Registration

8:30am - 9:00am — Opening: Welcome and opening speech
Location: Grand Ballroom

9:00am - 9:30am — Keynote speech 1: Extending Moore's Law with Advanced Packages by W.K.Wong(Xilinx)

9:30am - 10:00am — Keynote speech 2: : The evolution of packaging technology for mobile platform - Where we have been and where we are headed by Dr. Raj Pendse(Qualcomm)

10:00am - 10:30am — Coffee/Tea Breaks #1: Interactive session #1

10:30am - 11:50am

A-01: ID 283	A-02: ID 169	A-03: ID 127	A-04: ID 119	A-05: ID 154
A-06: ID 190	A-07: ID 203	A-08: ID 207	A-09: ID 188	A-10: ID 113
A-11: ID 256	A-12: ID 246	A-13: ID 128	A-14: ID 137	A-15: ID 123
A-16: ID 300	A-17: ID 205	A-18: ID 140	A-19: ID 167	A-20: ID 165
S-01: TSV/Wafer Level Packaging Location: Paradiso Room Chair: Avram Bar-Cohen	S-02: Interconnection Technologies Location: Cardinal Room Chair: Thomas Zerna	S-03: Material and Processing Location: Swallow Room Chair: Sungdong Kim	S-04: Mechanical modeling & simulation Location: Lyrebird Room Chair: Christopher Bailey	S-05: Quality, Reliability & FA Location: Falcon Room Chair: Stevan G Hunter

11:50am - 1:20pm — Lunch 01: EPTC 2016 Best Paper Awards, EPS Certification of Appreciation to EPTC 2017 Organizing Committee. Sponsor Appreciation
Location: Grand Ballroom

1:20pm - 1:50pm

Invited-01: Enhanced Bonding Technology for Hybrid Integration in 3D Packaging Technology : Dr. Guilian Gao(Xperi) Location: Paradiso Room	Invited-02: Packaging of Integrated Silicon Photonics devices : Electrical, Optical, Thermal Challenges and Application : Dr. Jun Su Lee(Tyndall National Institute) Location: Cardinal Room	Invited-03: Innovative Process and Equipment Technology Solutions for 3D SiP Packaging : Albert Lan(Applied Material) Location: Swallow Room	Invited-04: UV Laser Releasable Temporary Bonding Materials for Advanced Packaging technologies : Dr. Kenzo Ohkita(JSR) Location: Lyrebird Room	Invited-05: Trends in SIP and Placement Approaches : Chong Chan Pin(KNS) Location: Falcon Room

1:50pm - 3:10pm

B-01: ID 286	B-02: ID 121	B-03: ID 172	B-04: ID 175	B-05: ID 144
B-06: ID 280	B-07: ID 282	B-08: ID 206	B-09: ID 296	B-10: ID 208
B-11: ID 294	B-12: ID 141	B-13: ID 301	B-14: ID 227	B-15: ID 224
B-16: ID 273	B-17: ID 185	B-18: ID 220	B-19: ID 166	B-20: ID 237
S-06: Advanced packaging Location: Paradiso Room Chair: Martin Oppermann	S-07: Emerging Technologies Location: Cardinal Room Chair: Hideyuki Nasu	S-08: Equipment and Process automation Location: Swallow Room Chair: Eric Pabo	S-09: Material and Processing Location: Lyrebird Room Chair: Ramachandran Krishnan Trichur	S-10: Interconnection Technologies Location: Falcon Room Chair: Evelyn Napetschnig

3:10pm - 4:30pm — Coffee/Tea Breaks #2: : Exhibitor Presentation

4:30pm - 5:50pm

C-01: ID 193	C-02: ID 163	C-03: ID 112	C-04: ID 213	C-05: ID 146
C-06: ID 194	C-07: ID 164	C-08: ID 155	C-09: ID 162	C-10: ID 130
C-11: ID 201	C-12: ID 197	C-13: ID 135	C-14: ID 108	C-15: ID 180
C-16: ID 216	C-17: ID 295	C-18: Partner Conference Introduction	C-19: ID 231	C-20: ID 191
S-11: Mechanical modeling & simulation Location: Paradiso Room Chair: Santosh Kumar	S-12: Quality, Reliability & FA Location: Cardinal Room Chair: Karsten Meier	S-13: Thermal Characterization & cooling solutions Location: Swallow Room Chair: Marta Rencz	S-14: Emerging Technologies Location: Lyrebird Room Chair: Cher Ming Tan	S-15: Electrical Simulation & Characterization Location: Falcon Room Chair: Mihai Dragos Rotaru

6:30pm - 10:00pm	Conference Banquet

Date: Friday, 08/Dec/2017

Time					
8:30am - 9:00am	Invited-06: Wafer Bonding – An Enabling Technology for 3DIC, MEMS, BSI CIS, SOI, RF Filters, and More : Eric Pabo(EVG) Location: Paradiso Room	Invited-07: VCSEL-based Optical Interconnects and Their Packaging Technologies : Dr. Hideyuki Nasu(Furukawa Electric Co) Location: Cardinal Room	Invited-08: Temporary Bonding Materials for Fan-out Packaging Processes : Ram Trichur(Brewer Science) Location: Swallow Room	Invited-09: On-Chip Embedded Cooling of Power and Logic Components : Dr. Avram Bar-Cohen(Raytheon Corporation) Location: Lyrebird Room	Invited-10: Reliability Assurance: A Semiconductor Supplier's Perspective : Dr. Stevan G. Hunter(ON Semiconductor) Location: Falcon Room
9:00am - 10:20am	D-01: ID 104 D-06: ID 266 D-11: ID 305 D-16: ID 281 S-16: Interconnection Technologies Location: Paradiso Room Chair: Chan Pin Chong	D-02: ID 170 D-07: ID 288 D-12: ID 298 D-17: ID 214 S-17: Emerging Technologies Location: Cardinal Room Chair: Yan Cheong Chan	D-03: ID 230 D-08: ID 292 D-13: ID 181 D-18: ID 189 S-18: Material and Processing Location: Swallow Room Chair: Rajoo Ranjan	D-04: ID 171 D-09: ID 173 D-14: ID 192 D-19: ID 265 S-19: Thermal Characterization & cooling solutions Location: Lyrebird Room Chair: GONG YUE TANG	D-05: ID 198 D-10: ID 243 D-15: ID 268 D-20: ID 279 S-20: Quality, Reliability & FA Location: Falcon Room
10:20am - 11:10am	Coffee/Tea Breaks #3: Exhibitor Pressentation				
11:10am - 12:30pm	E-01: ID 124 E-06: ID 153 E-11: ID 159 E-16: ID 254 S-21: Materials and Processing Location: Paradiso Room Chair: Kenzo Ohkita	E-02: ID 275 E-07: ID 116 E-12: ID 222 E-17: ID 251 S-22: Advanced Packaging Location: Cardinal Room Chair: Jean Charbonnier	E-03: ID 247 E-08: ID 195 E-13: ID 218 E-18: ID 103 S-23: TSV/Wafer Level Packaging Location: Swallow Room Chair: Boo Yang Jung	E-04: ID 186 E-09: ID 196 E-14: ID 211 E-19: ID 228 S-24: Electrical Simulations & Characterization Location: Lyrebird Room Chair: Eldon Staggs	E-05: ID 236 E-10: ID 252 E-15: ID 125 E-20: ID 278 S-25: Mechanical Modeling & Simulations Location: Falcon Room Chair: Yong Han
12:30pm - 1:30pm	Lunch 02: Introduction of 20th Electronic Packaging Technology Conference Location: Grand Ballroom				
1:30pm - 2:00pm	Invited-11: Advanced eWLB FOWLP: Enabling Integrated Packaging Solutions : Dr. Seung Wook Yoon(STATS ChipPAC) Location: Paradiso Room	Invited-12: Highly accurate TSV, PWB and FO-PLP wiring fabication by plasma dry processes for interface : Dr. Yasuhiro Morikawa(ULVAC) Location: Cardinal Room	Invited-13: 10 Golden Rules of Chip-Package- Board Interactions : Dr. E.Napetschnig(Infineon Technologies Austria) Location: Swallow Room	Invited-14: Heterogeneous Integration Roadmap – Global Collaboration : William Chen(ASE, IEEE Electronic Packaging Society) Location: Lyrebird Room	Invited-15: Interconnect Reliability Assurance Through Electrical Testing : Prof. Tan Cher Ming(Chang Gung University, Taiwan) Location: Falcon Room
2:00pm - 3:20pm	G-01: ID 151 G-06: ID 209 G-11: ID 179 G-16: ID 174 S-26: Advanced Packaging Location: Paradiso Room	G-02: ID 304 G-07: ID 177 G-12: ID 250 G-17: ID 221 S-27: TSV/Wafer Level Packaging Location: Cardinal Room Chair: INDERJIT SINGH	G-03: ID 120 G-08: ID 105 G-13: ID 217 G-18: ID 114 S-28: Interconnection Technologies Location: Swallow Room Chair: Guilian Gao	G-04: ID 249 G-09: ID 244 G-14: ID 161 G-19: ID 253 S-29: Emerging Technologies Location: Lyrebird Room Chair: Jun Su Lee	G-05: ID 257 G-10: ID 245 G-15: ID 270 G-20: ID 233 S-30: Electrical Simulations & Characterization Location: Falcon Room Chair: Ranauld Perez
3:20pm - 3:50pm	Coffee/Tea Break #04: Interactive session #2				
3:50pm - 4:20pm	Keynote speech 3: Design tools and modelling for power electronics packages – current status and future challenges : Prof. Bailey(University of Greenwich)				

4:20pm - 4:40pm	**Closing Ceremony: Lucky Draw**

Date: Saturday, 09/Dec/2017

8:30am - 12:00pm	**Visit: Institution Visit**